Computing *Faster* *Without CPUs*

***GOAL*: Evaluate FPGA*-based Hypercomputer Potential for NASA Scientific Computations**

***TEAM*: Drs. Olaf Storaasli & Robert Singleterry, PIs**

Dave Rutishauser, Jarek Sobieski, Joe Rehder & Garry Qualls

William Fithian (Harvard), **Siddhartha Krishnamurthy** (VT)
Shaun Foley (MIT), **Neha Dandawate** (GS), **Kristin Barr** (JPMorgan)
Patrick Butler (VT), **Vincent Vance** (VT), **Robert Lewis** (Morehouse)

***PARTNERS*: Star Bridge Systems#**
NSA, USAF, MSFC

* **F**ield-**P**rogrammable **G**ate **A**rray (e.g. Polycom)
\# **NASA S**pace **A**ct **A**greement

William Fithian* (Harvard, Merit Scholar, Oracle Award)

Jumping into research world

By Katherine Martin
Daily Press

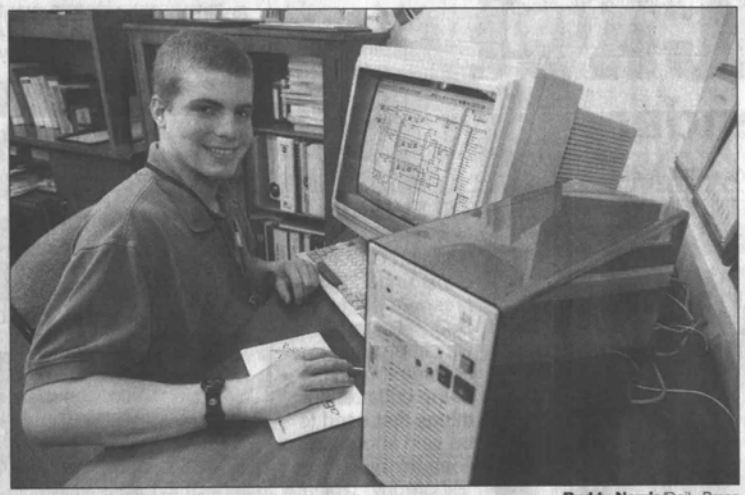
His deep voice carried over the banquet hall. The chatter throughout the room calmed and eventually everyone was silently listening to William Fithian's rendition of "Love and Marriage."

William, valedictorian of Poquoson High School, is a 17-year-old of many talents. He is a Presidential Scholar, co-captain of the varsity swimming team and aspiring a capella performer. Most recently he was selected for the Oracle Award, an academic honor given to nine students in the nation headed for a career in math or science.

William could have picked anyone in the state of Virginia to present his award. President George Bush presented the Texas winner's award. Michigan Gov. John Engler presented the award to that state's winner. Olaf Storaasli, a NASA Langley research scientist and William's Governor's School mentor for the past two years, presented Fithian's award.

"I feel really honored," Storaasli said. "William is just like another son to me. Of the many students I have mentored, William is the tops. We're expecting great things of him."

With a resume like William's, it would be hard to disagree with his mentor. With a perfect score on the SAT, 4.53 grade point average, captain and co-captain of various academic teams throughout his high school career and a varsity swimmer to boot, William will attend Harvard this fall.



Buddy Norris/Daily Press

William Fithian finds working at NASA on a Star Bridge computer challenging.

"You find your strengths and pursue them," he said. "The things you succeed in most are the things you love."

Wiliam's latest research interest at NASA has revolved around field programmable gate arrays, or FPGAs. These small gate arrays have the potential to be 100 to 500 times faster than conventional CPU processors because each program for the system customizes the FPGA chip nearly instantaneously.

FPGAs until recently have primarily been used in telecommunications. Robert Singleterry, a NASA research scientist, said the field needs people like William to incorporate this new technology for scientific applications.

"We have found the younger folk pick up the program a lot better than the older folks," Singleterry said.

William worked with the new system using a graphical programming language called VIVA, a language invented by Star Bridge Systems Inc. Storaasli said William picked up the language in a matter of two meetings.

"Working on a program can be frustrating when it isn't working and you don't know why," William said. "I love the problem-solving aspect. Computer science is a lot like math. It's problem solving. You write a program, run it and debug it."

The 17-year-old said he owes his interest in research to the Governor's School. During the junior year, local scientists mentor each Governor's School participant. William said Storaasli's reputation preceded their initial meeting. "I heard Dr. Storaasli was an excellent mentor, so I e-mailed him about it and asked if he would be my mentor," he said. "He is first and foremost my motivation for going into scientific research."

Storaasli said some students can be a lot of work. William is an exception. "William and others are self-starters. Show them the ropes and let them have freedom to try out their ideas," Storaasli said. "William is already like a NASA researcher, often surpassing what you expect."

Ellen Fithian, William's mother, said she is thankful for Storaasli's influence. "It's been nice for William to have this opportunity," she said. "Having Olaf as his mentor is important because we don't have a computer-science background."

Ned Carr, executive director of New Horizons Regional Education Center, said William's mentoring experience is what the program aims for. "It prepares students to make real unique contributions to society," Carr said. "When I watched William's (mentorship) presentation (with Storaasli and Singleterry), it was like a discussion between three colleagues."

William leaves for Harvard this fall. While he said he doesn't think he will have a chance to work with FPGAs, he does want to contribute to the field of computer science. "I want to create new software and hardware," he said. "Instead of seeing computers as a tool, I want to program them into something they haven't done before."

While William said he doesn't know what that might be, he did say he plans to return to Virginia during the summers to work with NASA via their summer internship program for college students.

Katherine Martin is a free-lance writer for the Daily Press.

William Fithian

WHO: One of nine high school seniors in the nation to receive the Oracle Award. To date, he has received $14,500 in scholarships. He will be attending Harvard this fall.
AGE: 17
RESIDENCE: Poquoson, attending Poquoson High School
FAMILY: Father, Tom; mother, Ellen; sister Rachel, 22, attending Princeton University; sister Diana, 20, attending Brown University; and brother Brian, 14
ACHIEVEMENTS: National Merit Scholar, varsity swimmer, Presidential Scholar, USA Math Olympiad participant, president of the National Honor Society at Poquoson High

*NASA-NHGS mentorship '00-'02

Viva 2.0

Project Executable Sheet Edit View System Tools Help

FPGA: *New Computing Paradigm*

Traditional CPU *Reconfigurable FPGA*

Sequential: 1 operation/cycle **Parallel**: Inherent

Fixed gates & data types **Dynamic** gates & data types

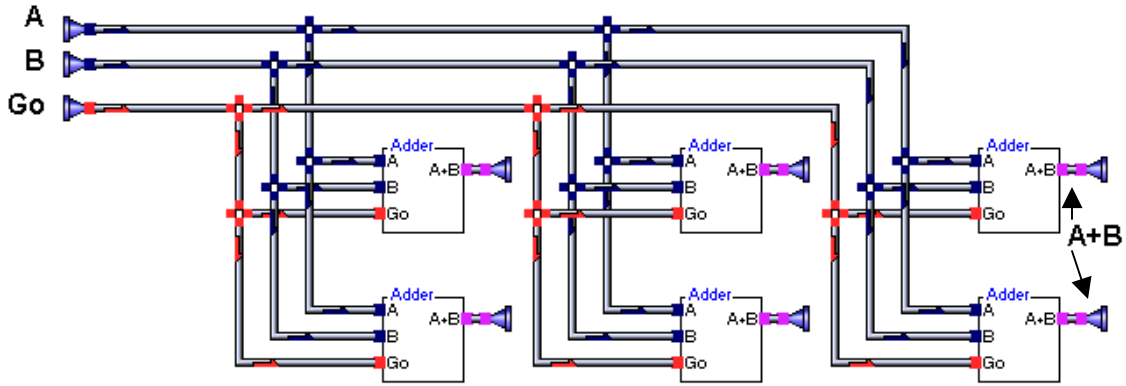
Wasteful: 99% gates idle/cycle **Efficient**: Optimizes gates to task

yet all draw power

Software: Text

```
do i = 1, billion
    c= a+b
end do
```

Gateware: VIVA Icons & Transports



392+ MFLOPS/64 MHz FPGA

26 MFLOPS/250 MHz SGI

3.92+ GFLOPS/10 FPGA board

New Project
MetaLib

Basic Data Sets
COM Data Sets
Primitive Objects
Input
Output
$Select
AND
DeRef
INVERT
OR
Ref
Release
Text
Composite Objects
Control
Convert
DataInfo
ExposeCollect
Gates
I/O
Math
Memory
Mux
Registers
Shifting
TestSheets

I2ADL Editor | Data Set Editor

Project | System | COM

Start C:\Viva Viva 2.0 2:58 PM

VIVA: *Gateware Development Tool*

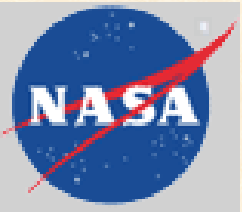
What: Simple tool to configure FPGAs (VHDL cumbersome)

How: Transforms high-level graphical code to logic circuitry

Why: Achieve near-ASIC speed (w/o chip design)

Growth in VIVA Capability

VIVA 1 (Feb '01)	*VIVA2 (July '02)*
NO Floating Point	Extensive Data Types
NO Scientific Functions	Trig, Logs, Transcendentals
NO File Input/Output	File Input/Output
NO Vector-Matrix Support	Vector-Matrix Support
Access to One FPGA	Access to Multiple FPGAs
Primitive Documentation	Extensive Documentation
Weekly Changes	Stable Development
Frequent "bugs"	Few "bugs"

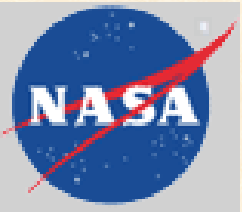


Langley Hypercomputers

10 FPGAs each

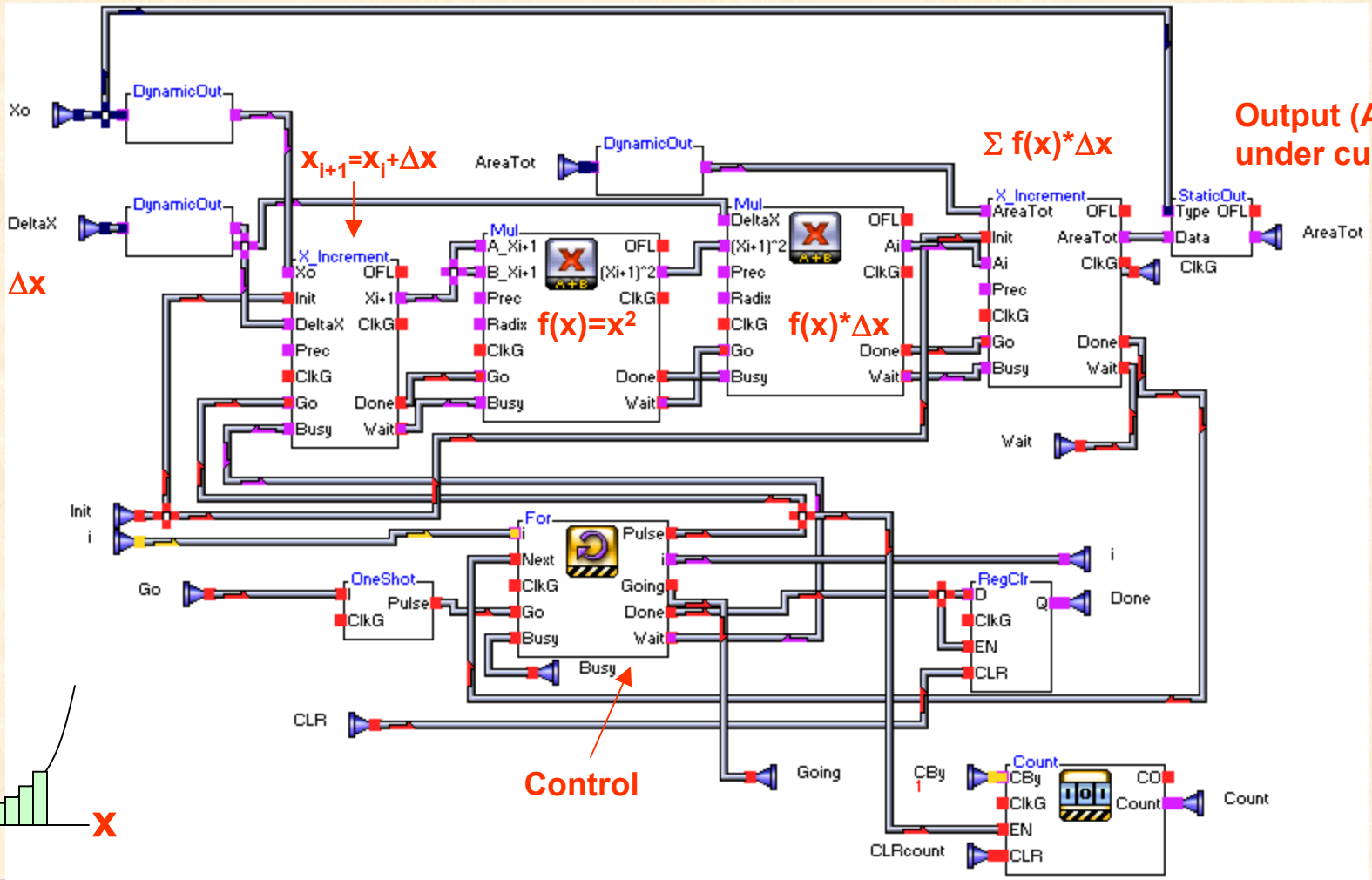
Langley Algorithms Developed*

- **Matrix Algebra**: Vectors, Matrices, *Dot Product*
- **Factorial** => Probability: Combinations/Permutations AIRSC
- **Cordic** => Transcendentals: sin, log, exp, cosh…
- ***Integration* & Differentiation** (numeric)
- ***Matrix Equation Solver***: [A]{x} = {b} via Gauss & Jacobi
- **Dynamic Analysis**: $[M]\{\ddot{u}\} + [C]\{\dot{u}\} + [K]\{u\} + NLT = \{P(t)\}$
- **Analog Computing**: digital implementation
- **Nonlinear Analysis**: "Analog" simulation avoids NLT solution development time



* In *AIAA* & *Military & Aerospace Programmable Logic Device (MAPLD)* papers

Numeric Integration

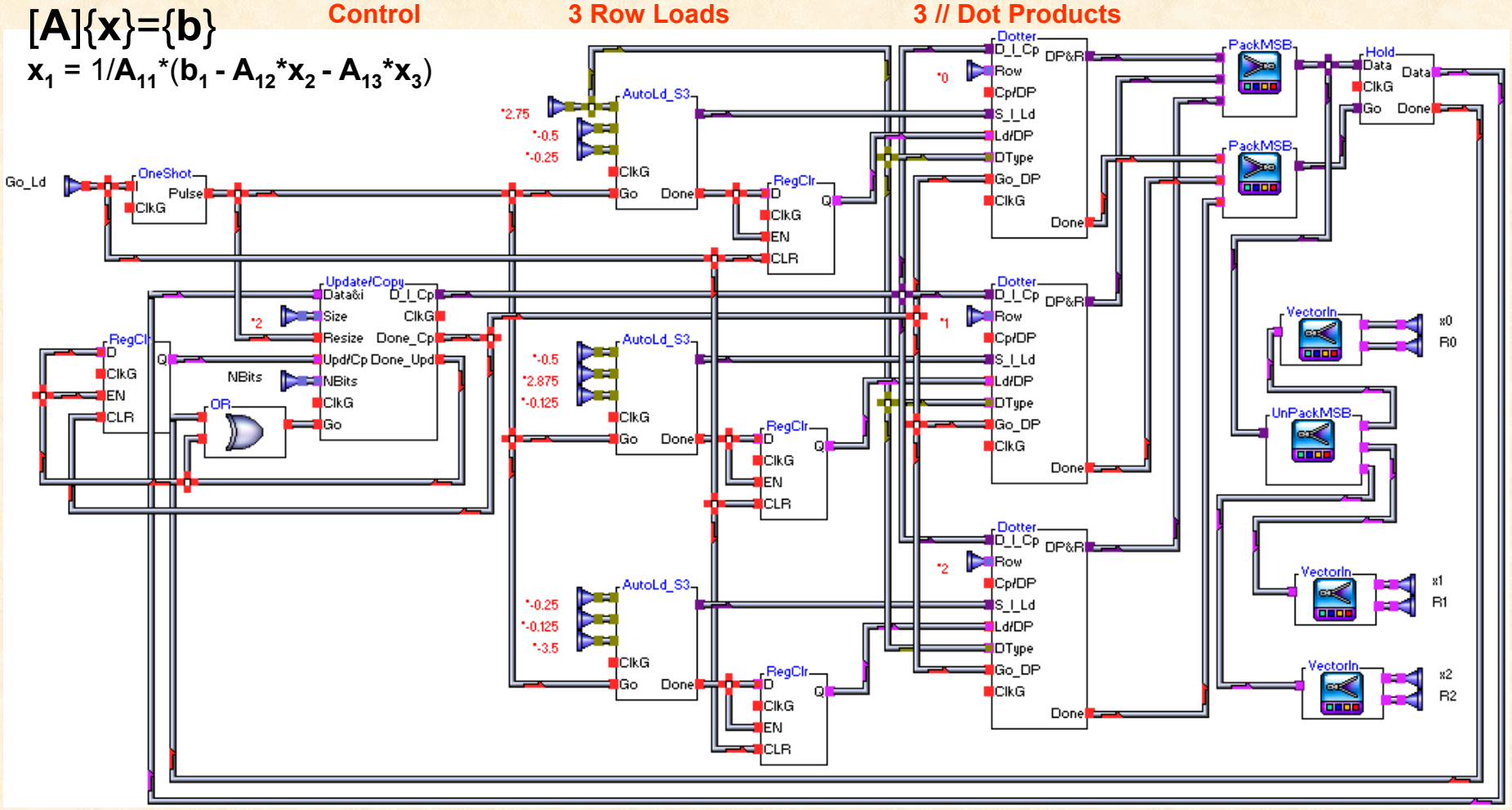


VIVA Sparse Matrix Equation Solver

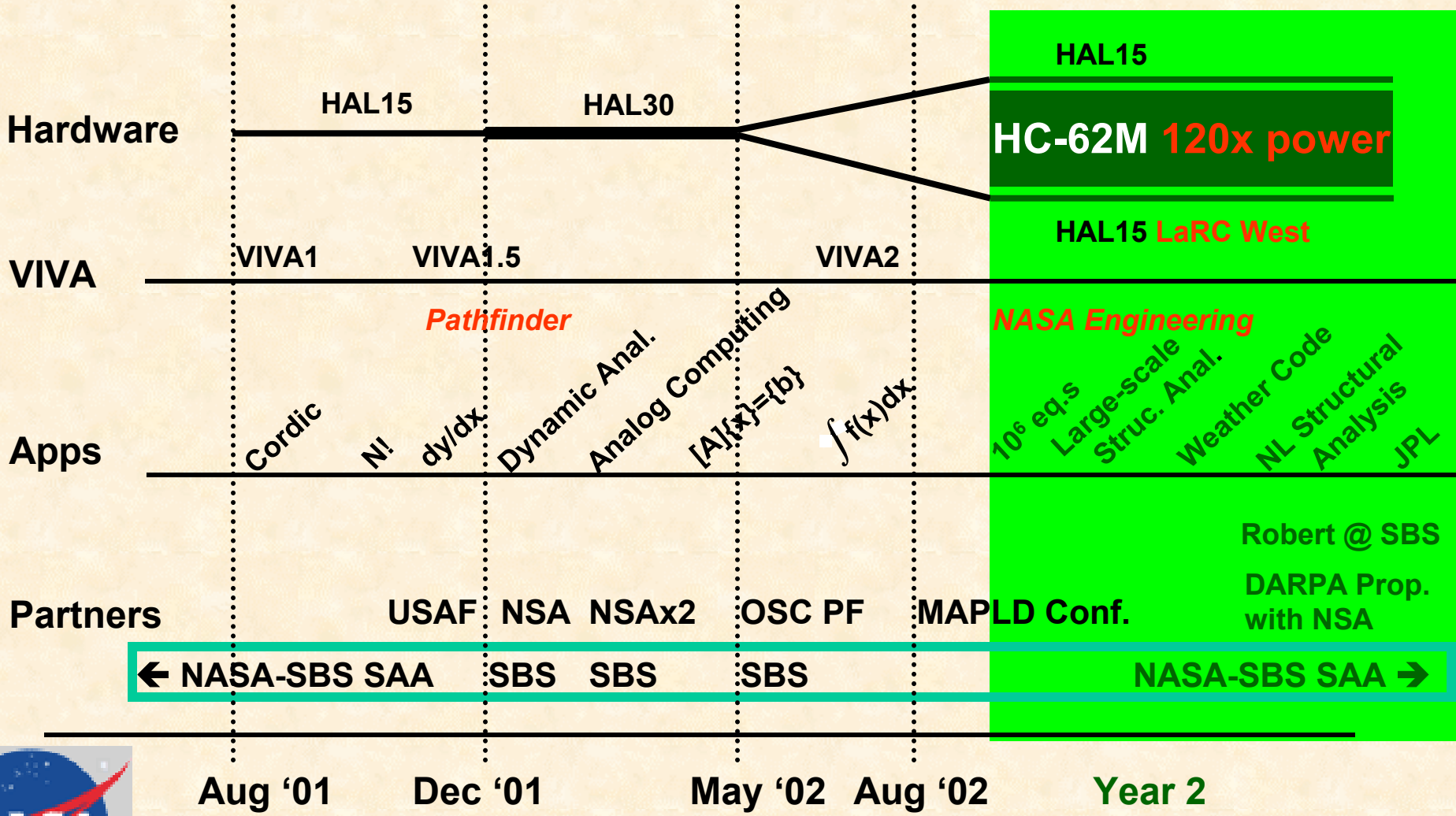
Jacobi Iterative (3x3 Demo)

$[A]\{x\}=\{b\}$

$x_1 = 1/A_{11}*(b_1 - A_{12}*x_2 - A_{13}*x_3)$



Progress - Roadmap



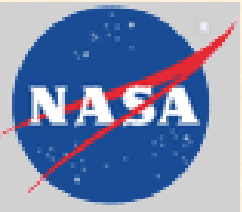
Year 2: Exploit Latest FPGAs

Rapid Growth in FPGA Capability

	FPGA (Feb '01)	FPGA (Aug '02)
Xilinx FPGA	XC4062	XC2V6000
Gates	62K	6 million (97x)
Multiplies in H/W	0	144 (18x18)
Clock Speed MHz	100	300 (3x)
Memory	20Kb	3.5 Mb (175x)
Memory Speed	466 Gb/s	5 Tb/s (11x)
Reconfigure Time	100ms	40ms (2.5x)
GFLOPS	0.4	47 (120x)
Total GFLOPs	**4** (10 FPGAs)	**470** (10 FPGAs)

Plans:

- Millions of Matrix Equations for Structures, Electromagnetics & Acoustics
- Rapid Static & Dynamic Structural Analyses
- Cray Vector Computations in Weather Code (VT PhD)
- Robert on Administrator's Fellowship at Star Bridge Systems
- Joint proposals with NSA & DARPA
- Simulate advanced computing concepts using VIVA
- Collaborate with SBS to expand VIVA libraries
- Influence VIVA development to meet NASA application needs
- Expand FPGA applications for NASA programs



Summary

What We've Learned

We like FPGA promise – accomplished much

Hardware: Tested 2 futuristic FPGA systems

FPGAs: Inherently //, flexible, efficient, & fast

VIVA: Powerful & growing (tailored to NASA needs)

Applications: Diverse "pathfinder" algorithms developed

FPGA technology: Advancing dramatically

Speed: Year 1: 4 GFLOPS => Year 2: 470 GFLOPS

Future: Year 2 promises "cutting edge" innovations

comprehensive NASA engineering applications